

## M. HIGH RELIABILITY TESTING

### BURN IN

Dielectric formulations and chip capacitors are often tested for reliability under voltage and temperature for specified time periods, a process referred to as “burn in” or “voltage conditioning”. Specifications applicable to burn in of MLC capacitors are MIL-C-55681, MIL-C-123 and MIL-C-49467. Burn in may also be performed to particular customer specifications. The test voltage is usually twice the working voltage rating of the device, at 85°C or 125°C for a duration of 96 hours, 100, or 168 hours test time, typically.

Burn in is accomplished by loading of units in a fixture, usually a PC board which contacts to a power supply with access to the rear wall of a standard oven. Units are monitored for current leakage under voltage and temperature stress either individually or in tandem, with measurement of leakage from a group of a hundred units, typically. Tandem testing is more rapid and used to mass produce burned in product. Sophisticated equipment is used with automatic data monitoring to record the location and time of test cycle failures.

Chip capacitors destined for high reliability testing are often designed with an added margin of safety, namely maximization of the dielectric thickness, and tested extensively for electrical properties prior to burn in (capacitance, DF and insulation resistance). These data are compared to post life test data for evaluation of the reliability of the components.

### FAILURE MODES

Capacitors which fail burn in usually lose resistivity at the elevated temperature and voltage, either catastrophically, or gradually with time, resulting in IR rejects. The failure rate is usually inversely proportional with time, i.e. more failures are observed earlier in the test cycle.

Excellent electrical properties at 25°C may not guarantee good performance during life test (hence the purpose of the test), for several reasons:

Poor dielectric properties: Ceramic dielectrics with elevated insulation resistance at room temperature may nevertheless experience excessive loss of resistivity at 125°C due to improper formulation, whereby charge carriers become mobile and develop a leakage current, decreasing the insulation resistance below specifications.

Poor microstructure: Voids, cracks or delaminations within the chip structure undermine the intrinsic resistivity of the material, providing leakage paths conducive to failure. This does not imply, however, that units which survive life testing are always free of microstructural defects. Experience has shown that despite rigorous testing, units with delaminations may still perform adequately,

while failures may be observed in units with apparent “excellent” microstructure. This is due to the fact that delaminations may often affect only the plane of the electrodes, without serious deterioration of the dielectric between electrodes of opposite polarity. Cracks, voids or impurities which straddle the electrode array are more conducive to eventual degradation under voltage and temperature. The latter defect may be microscopic in magnitude, and not easily observed or located within the chip microstructure, which may otherwise appear quite normal.

A second failure mode independent of the above, is degradation of the capacitance value and/or dissipation factor of the chip capacitor, i.e. post burn in data does not correlate well to the original electrical test data.

Class I dielectrics, which are non-ferroelectric, do not exhibit capacitance aging with time, temperature or voltage. Any burn in induced capacitance change in Class I chips is associated with mechanical failure, such as cracking which isolates electrode layers. Class II dielectrics, however, may display capacitance and dissipation factor variations after burn in without mechanical failure, as these dielectrics are time, temperature and voltage dependent. Most notably, the accelerated aging of the dielectric constant under burn in conditions must be considered for proper interpretation of results; units under test may be exposed to three very different aging scenarios, depending on the method used to terminate the life test. The following three conditions assume that pre-burn in data was performed on de-aged units:

- a. The voltage is removed while the units are at temperature, and temperature is maintained with no bias for a minimum of one hour. Under this condition, total de-aging of capacitors occurs, and units will display minimal (positive or negative) capacitance change with respect to the original pre-burn in values.
- b. Capacitors remain under dc bias while the oven is permitted to cool to room temperature. This in effect is a voltage conditioning process and the units will therefore age with respect to the original test data, e.g. -7.0%  $\Delta C$ .
- c. The voltage is removed at the burn in temperature and the units subsequently taken from the oven and allowed to air cool to room temperature. In this case, the units do not fully age during the cooling cycle, as in example (b), nor do they totally de-age as in (a) above. The components thus experience a partial aging only, e.g. -3.5%  $\Delta C$ .

The % $\Delta C$  values given as examples for the post burn in data above are typical of some Mid-K dielectrics. High-K less stable dielectrics may experience more radical capacitance changes, as these materials have an aging rate of 5% per decade hour typically, three times the average rate of X7R formulations. These considerations clearly indicate that procedure (a) only should be followed for termination of the life test for proper evaluation of performance of Class II dielectrics.

In addition to burn in, high reliability often involves other performance tests, as outlined in Table L-2, per MIL-C-55681 or to customer specifications. The most common of these additional tests are dielectric withstanding voltage and insulation resistance at elevated temperature, voltage-temperature limits, thermal shock, solderability and solder leach resistance of the chip capacitor termination. In addition, strict visual and mechanical examination of the product may be required, including Destructive Physical Analysis (DPA). The various group categories of high reliability testing applicable to MIL specifications are outlined in Table M-1. Any or all of the Group tests may be specified by customers requiring high reliability product.

TABLE M-1  
HIGH RELIABILITY TEST PROCEDURES

Specification	MIL-C-55681	MIL-C-123B
GROUP A	Voltage Conditioning IR @ Elevated Temperature Visual & Mechanical Inspection ESR, when Specified Solderability	Thermal Shock Voltage Conditioning Visual & Mechanical Inspection, Destructive Physical Analysis
Specification	MIL-PRF-49467A (High Voltage)	MIL-PRF-39014F (Leaded Devices)
GROUP A	Thermal Shock Voltage Conditioning Partial Discharge Radiographic Inspection Mechanical Examination Visual Examination Solderability	Thermal Shock Voltage Conditioning Radiographic Inspection Mechanical Examination Visual Examination Solderability
GROUP B	Environmental and Life Tests performed for qualification, or to attain Established Reliability, applicable to any specification, if required.	
GROUP C		