

K. TEST PARAMETERS AND ELECTRICAL PROPERTIES

Electrical behavior of ceramic chip capacitors is strongly dependent on test conditions, notably temperature, voltage and frequency, for reasons explained in Sections F through I. This dependence on test parameters is more notable with Class II ferroelectric dielectrics, and negligible or more easily predictable with Class I formulations. For this reason, certain standards of measurement have been established in the industry, with the appropriate limits of performance for any given electrical property and dielectric characteristic.

TEMPERATURE DEPENDANCE

Temperature Coefficient (Capacitance-Temperature Dependence): The variance of capacitance with temperature is used to classify dielectric formulations, as described in Section J. In general, it is found that materials with higher dielectric constants at 25°C display greater change with temperature, on the hot or cold side of reference, as the higher K materials are based on formulations which shift the sharp Curie peak to room temperature. Lower K dielectrics, which are formulated to suppress and broaden the Curie peak over temperature, display more stability, as intended. This effect is clearly evident in the curves of Figure J-3 for X7R and High-K dielectrics.

The temperature coefficient (T.C.) is expressed in ppm/°C for Class I type ceramics, and as %ΔC for Class II. Measurements are obtained by maintaining chip capacitor samples under controlled temperature conditions in a temperature or “T.C.” chamber, while accurate readings of capacitance are made at various temperatures, usually -55°C, 25°C and 125°C. Accuracy of fixtures and test equipment is obviously important, especially when measuring lower capacitance values where small changes in ppm/°C may provide only a fraction of a picofarad in capacitance change from the reference value. Care must also be exercised when measuring higher value Class II dielectrics, due to the de-aging property of these materials. The de-aging of samples at the hot stage of the measurements may result in erroneous T.C. calculations; it should be a practice to de-age these capacitors for a minimum of one hour before T.C. measurements are made.

The temperature coefficient for Class I dielectrics is calculated in ppm/°C for any given temperature range, using the following expression:

$$\text{T.C. (ppm/°C)} = [(C_2 - C_1) / C_1(T_2 - T_1)]10^6$$

where: C_1 = capacitance @ T_1
 C_2 = capacitance @ T_2
and $T_2 > T_1$

Examples: Capacitance measurements at temperature are as follows:

-55°C, 1997 pF
25°C, 2000 pF
125°C, 2004 pF

Computation of the T.C. slope for the -55°C to 25°C range:

$$\text{T.C.} = [(2000-1997) 10^6] / 1997[25-(-55)] = 18.7 \text{ ppm/}^\circ\text{C}$$

Computation of the T.C. slope for the 25°C to 125°C range:

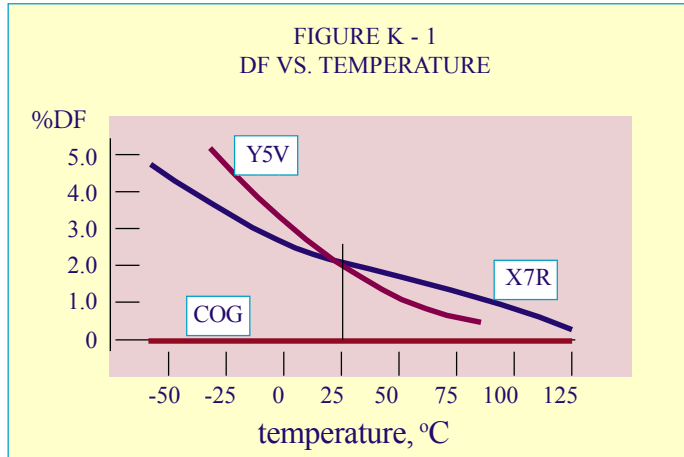
$$\text{T.C.} = [(2004-2000) 10^6] / 2000(125-25) = 20.0 \text{ ppm/}^\circ\text{C}$$

The temperature coefficient for Class II dielectrics is reported as the percent change from the room temperature measurement, as the variations observed are several orders of magnitude greater than those for the linear dielectrics.

The acceptable limits for any given dielectric characteristic are specified in the EIA 198 specification, as shown in Tables J-1 and J-2.

Dielectric Loss and Temperature: Class I dielectrics display only negligible change in dissipation factor with temperature over the standard -55°C to 125°C temperature range. Industry standards require that at 25°C the DF is not to exceed .001 (0.1%) for standard linear dielectrics (COG-NPO) and not to exceed .002 (0.2%) for the extended T.C. series of dielectrics.

Class II dielectrics show a general decrease of DF with temperature, notably at or near the Curie Point of the material. Above the Curie Point, the energy consuming ferroelectric domains no longer operate and internal losses are minimized. At temperatures below the Curie Point, the domain relaxation processes for any given Vac signal are activated, and energy loss is reflected in an increase in the dissipation factor. The complexity of the ceramic microstructure and the resultant multiple Curie Points of the aggregate polycrystalline components in any given formulation do not permit a clear prediction of DF behavior with temperature, other than the fact that DF is inversely proportional to temperature. Industry standards for Mid-K dielectrics, such as X7R, require that at 25°C the DF not exceed .025 (2.5%). High-K dielectrics, such as Z5U and Y5V, are often specified with a maximum DF of .030 (3.0%) at 25°C. Typical DF curves with temperature are shown in Figure K-1 for several dielectrics.



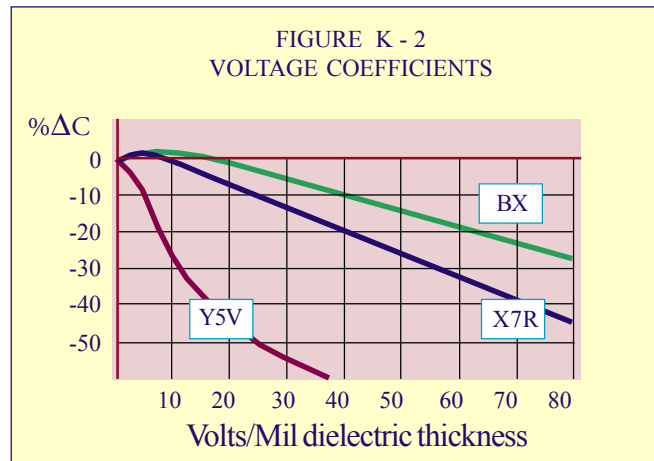
Insulation Resistance and Temperature: The properties which give rise to the insulation resistance of dielectrics were outlined in Section G-1. As described in that portion of the text, the mechanisms of conduction are temperature dependent, and leakage of current increases with temperature, as added thermal energy increases the diffusion of charge carriers. It is found that in general the IR of most dielectrics at 125°C decreases by a factor of one to two orders of magnitude from the 25°C measurement. Industry standards require that the IR readings at 125°C exceed 100 ohm-Farad, (10% of the values shown in Table G-1).

Dielectric Strength and Temperature: The dielectric strength of insulators is inversely proportional to temperature, as heat lowers the intrinsic resistivity of the material as discussed previously. As a general rule, a properly designed capacitor of sound construction should withstand the normal 25°C dielectric withstanding “flash” voltage at 125°C.

VOLTAGE (VDC) DEPENDANCE

Vdc Coefficient: Ferroelectric Class II formulations are sensitive to dc voltage. In all cases an eventual decrease in dielectric constant occurs with dc bias, which is more severe with dielectrics of higher dielectric constant. This behavior is attributed to a constraint of the dc voltage on the response of the polarizing mechanisms which give rise to the dielectric constant of the material.

The curves of Figure K-2 are data for various formulations. The curves show the expected capacitance change with increased volts/mil dc bias. As is evident from these data, consideration of the effect of dc bias requires knowledge of the construction of the capacitor, as the thickness of the individual dielectric layers will determine the volts/mil loading of the device during operation. In effect capacitors of identical capacitance value and voltage rating may behave quite differently depending upon internal construction.



Consider the following examples:

a. Capacitor of 0.1 mfd, constructed of 20 layers, 1.0 mil thick, X7R dielectric, rated at 50 volts: The predicted capacitance change, based on the data of Figure K-2, is -25%, as the dielectric is stressed at 50 volts/mil when operating at 50 Vdc.

b. Capacitor of 0.1 mfd, built with the same dielectric, but constructed with 30 layers 1.5 mils thick. At 50 Vdc. operation, however, the dielectric layers experience only 33 volts/mil, and the predicted capacitance change is therefore reduced to -15%.

c. Capacitor of 0.1 mfd, built with 40 layers of 2.0 mil dielectric will experience only 25 volts/mil at 50 Vdc, and the predicted capacitance change is further reduced to -10%. The effect is of considerable importance in the design of capacitors intended to meet characteristics which require that the combined temperature and voltage coefficients (TVC) not exceed a certain ΔC over the operating temperature range, at working voltage. Assuming that a dielectric is available with T.C. characteristics well within the $\pm 15\%$ max ΔC , the manufacturer need only be concerned with the negative contribution of the voltage coefficient. For the examples stated above, and assuming that the T.C. of the dielectric utilized varies typically $\pm 7\%$ maximum, the maximum TVC for the three examples are as follows:

	T.C.	VC	Max. TVC	Characteristic
a.	+7%-7%	-25%	(+7%-32%)	X7R only
b.	+7%-7%	-15%	(+7%-22%)	X7R and BX (marginal)
c.	+7%-7%	-10%	(+7%-17%)	X7R and BX

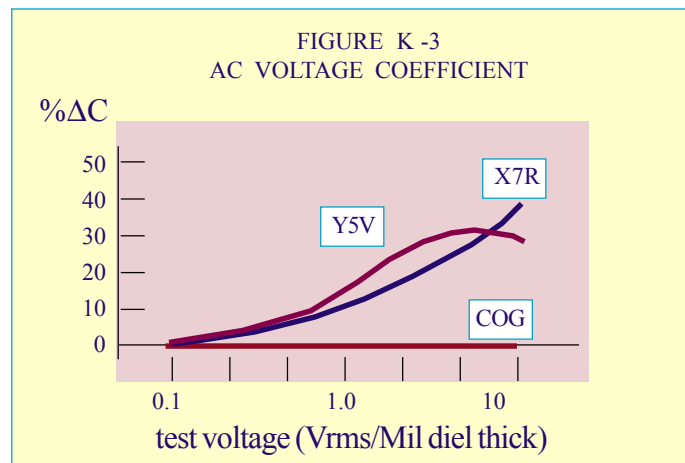
Voltage Conditioning - Aging Effects: Class II dielectrics experience an accelerated aging effect when stressed by dc voltage, as briefly described in Section G-3. This effect is evident even at room temperature, and is more dominant at higher voltage and with dielectrics with elevated dielectric constant. In the manufacture of close tolerance ($\pm 5\%$) Mid-K dielectrics, or high voltage units, the product is usually reheated after IR or dielectric withstanding voltage testing, to maintain capacitance tolerance and establish a fresh aging cycle. X7R units may derate as much as 3% in capacitance after dc withstanding voltage testing at 300 volts/mil.

DF and dc Voltage: Class II dielectrics experience a decrease in dielectric loss with increasing voltage. The DF may be reduced by a factor of 75% at 100 volts/mil bias for X7R dielectric.

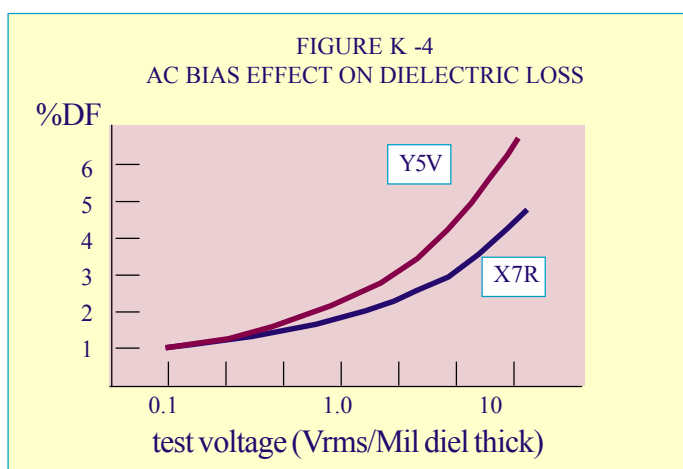
AC VOLTAGE DEPENDANCE

AC Voltage Coefficient: Class II dielectrics are fairly sensitive to test voltage, which can create significant changes in the measured dielectric constant, as illustrated in Figure K-3. The response to AC voltage always shows an increase in dielectric constant with the AC signal, with the higher K dielectrics responding more readily, until some threshold voltage value is reached where the effect reverses. Class I dielectrics, operating in the paraelectric state, display negligible or only limited response to the AC bias.

Industry standards specify a test voltage of $1.0 \pm 0.2 V_{rms}$ for all dielectrics with the exception of some High-K less stable Class II bodies which are specified by manufacturers at 0.1 or 0.5 V_{rms} , typically. Application of these materials at other voltages therefore presents correlation problems, even at low voltage stress (under 5 V_{rms}/mil) as evident from the data of Figure K-3. As occurs with the interpretation of dc voltage coefficient, the situation is further complicated by the added variable of capacitor design, i.e. dielectric thickness of the individual layers.



Dielectric Loss and AC Voltage: The increase of dielectric constant with AC test voltage is accompanied by a marked increase in the dissipation factor, as illustrated in Figure K-4. The multilayer construction of chip capacitors, with thin dielectric layers, precludes application in circuitry with large AC voltage and high current, as dielectric losses become quite significant between 5 and 20 Vrms/mil stress.



FREQUENCY DEPENDANCE

The close interrelationship of frequency and dielectric polarization and dielectric loss was described in some detail in Sections F-2 and F-4. Increased frequency of an applied field results in a decrease of the measured capacitance value. This dependence is due to the inability of some of the polarizing processes to respond to the ever faster polarity reversals of the field, such that the net contribution of polarization to the dielectric constant of the material is reduced, and the dielectric loss is increased. These effects are common to all the dielectric groups, but are more predominant in the ferroelectric formulations which display large ionic polarization. Typical curves for capacitance and dissipation factor versus frequency are illustrated in Figures K-5 and K-6.

AGING -TIME DEPENDANCE

The phenomenon of ferroelectric dielectric aging is described in Section G-3. Restraints on the % per decade hour aging rates are usually specified by users of chip capacitors. X7R is expected to age less than 2.5%/decade hour, and most dielectrics within this characteristic typically have aging rates from 0.8% to 2.0% per decade hour. The High-K aging specification is more liberal by necessity; an aging rate of 5% per decade hour is considered normal.

Many of the Class II dielectrics may also display aging of the dissipation factor, an effect more predominant with High-K formulations.

